a bias transistor having a base, emitter, and collector;

wherein the bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the base and collector of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

Remarks

Claims 1, 9-17, and 21-22 are presently active.

Informalities are corrected in claims 1, 17, 21, and 22.

In the office action dated 15 November 2002 ("Office Action"), claims 9, 10, and 13 were rejected under 35 U.S.C. §102(e) as being anticipated by Williamson, U.S. patent 6,194,973B1 ("Williamson"); claims 1, 9, and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by Hariton, U.S. patent 5,926,064 ("Hariton"); claims 11, 12, and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hariton; and claims 13-17 and 22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art Fig. 2 and in view of Hariton.

35 U.S.C. §102(e) rejection of claims 9, 10, and 13 in view of Williamson

Claims 9, 10, and 13 include the limitation that the sources and drains of the first and second field effect transistors, and the drain and gate of the third field effect transistor, are all connected to each other. As an example, see Fig. 4 of the present application, where it is seen that the sources and drains of transistors 402 and 404, and the gate and drain of transistor 406, are all connected to each other. But the circuit taught in Fig. 9 of Williamson is very different from that which is claimed. The sources and drains of transistors MCX0 and MCX1 are connected to each other, but they are not connected to the gate and drain of transistor M2. Furthermore, the gate and drain of transistor M2 are not connected to each other.

Consequently, Applicant believes that claims 9, 10, and 13 are not anticipated by Williamson.

35 U.S.C. §102(b) rejection of claims 1, 9, and 10 in view of Hariton

Claim 1 recites the limitation that the sources and drains of the first and second field effect transistors and the gate and drain of the bias transistor have a substantially same voltage potential. But nowhere is it taught in Hariton that (referring to Fig. 5 of Hariton) the gate and drain of bias transistor 505 is at the same voltage as the sources and drains of transistors 302 and 303.

As discussed above, claims 9 and 10 include the limitation that the sources and drains of the first and second field effect transistors, and the drain and gate of the third field effect transistor, are all connected to each other. But in Fig. 5 of Hariton, the drain and gate of transistor 505 are not connected to the sources and drains of transistors 302 and 303.

Consequently, Applicant believes that claims 1, 9, and 10 are not anticipated by Hariton.

35 U.S.C. §103(a) rejection of claims 11, 12, and 21 in view of Hariton

For the same reasons as given above regarding the 35 U.S.C. §102(b) rejection of claims 1, 9, and 10 in view of Hariton, Applicant believes that claims 11, 12, and 21 are patentable over Hariton.

35 U.S.C. §103(a) rejection of claims 13-17 and 22 in view of Applicant's Fig. 2 and Hariton

Fig. 2 of the present application is cited only because it teaches a communication device with an amplifier having a capacitor connected as shown. (See previous office action of February 2002, page 4, item no. 8.) However, for the same reasons as given above regarding the 35 U.S.C. §102(b) rejection of claims 1, 9, and 10 in view of Hariton, Applicant believes that claims 13-17 and 22 are patentable over Applicant's Fig. 2 and Hariton.

Respectfully submitted,

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